

CLAIMS

1. A semiconductor device comprising:

5 a high-breakdown-voltage regulator configured to operate at a high input voltage;

a reference voltage generating circuit structured as a low-breakdown-voltage component and configured to receive an output voltage from the high-breakdown-voltage regulator to generate a reference voltage;

10 a differential amplifier circuit structured as another low-breakdown-voltage component and configured to receive the output voltage from the high-breakdown-voltage regulator and the reference voltage from the reference voltage generating circuit to produce a drive voltage;

15 an output driver structured as a high-breakdown-voltage component and configured to operated based on the drive voltage; and

resistors connected in series to the output driver to divide an output voltage of the output driver and feed the divided voltage back to the differential amplifier circuit.

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2. The semiconductor device of claim 1, wherein the high-breakdown-voltage output driver and the low-breakdown-voltage components are MOS transistors with gate oxide films having a first thickness.

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3. The semiconductor device of claim 2, wherein the high-breakdown-voltage regulator is structured by a high-breakdown-voltage MOS transistor with a gate oxide film having a second
5 thickness greater than the first thickness.

4. The semiconductor device of claim 1, wherein the output driver is a P-channel MOS transistor, the semiconductor device further comprising a diode inserted between the gate and the source of
10 the P-channel MOS transistor and having a reverse breakdown voltage lower than an oxide breakdown voltage of the P-channel MOS transistor.

5. The semiconductor device of claim 1, wherein the output driver
15 is an N-channel MOS transistor, the semiconductor device further comprising a diode inserted between the gate and the source of the N-channel MOS transistor or between the gate and the ground and having a reverse breakdown voltage lower than an oxide breakdown voltage of the N-channel MOS transistor.

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6. The semiconductor device of claim 1, wherein the output driver is a P-channel MOS transistor, the semiconductor device further comprising a constant current inverter inserted between the differential amplifier circuit and the output driver, the
25 constant current inverter comprising:

a constant current circuit connected between a power supply line and the output driver; and

a MOS transistor controlled by the drive voltage output from the differential amplifier circuit.

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7. The semiconductor device of claim 1, wherein the output driver is a P-channel MOS transistor, the semiconductor device further comprising a constant current inverter inserted between a power supply line and the output driver, the constant current inverter

10 comprising:

a first N-channel MOS transistor to which the reference voltage generated by the reference voltage generator is supplied;

a first P-channel MOS transistor connected in series to the first N-channel MOS transistor to produce a constant current;

15 a second P-channel MOS transistor defining a constant current circuit under a current mirror configuration; and

a second N-channel MOS transistor to which the drive voltage output from the differential amplifier circuit is supplied.

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8. A semiconductor device comprising:

a reference voltage generating circuit configured to generate a reference voltage;

25 a differential amplifier circuit configured to receive the reference voltage and generates a drive voltage;

an output driver configured to operate based on the drive voltage;

resistors connected in series to the output driver to divide an output voltage of the output driver and feed the
5 divided voltage back to the differential amplifier circuit; and
a constant current circuit inserted between a power supply line and a combination of the reference voltage generating circuit and the differential amplifier circuit.

10 9. The semiconductor device of claim 8, wherein the constant current circuit is structure by a depression-mode N-channel or P-channel MOS transistor.

10. The semiconductor device of claim 8, wherein the constant
15 current circuit is structured by an enhancement-mode N-channel or P-channel MOS transistor.

11. The semiconductor device of claim 8, wherein the constant current circuit is structure by multiple MOS transistors
20 connected in series to form a multi-stage constant current circuit.